(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 March 2003 (13.03.2003)

PCT

(10) International Publication Number
WO 03/021656 A2

(51) International Patent Classification[7]: H01L 21/316

(21) International Application Number: PCT/EP02/09259

(22) International Filing Date: 19 August 2002 (19.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/944,918 31 August 2001 (31.08.2001) US

(71) Applicant *(for all designated States except US)*: **INFINEON TECHNOLOGIES AG** [DE/DE]; St.-Martin-Str. 53, 81669 München (DE).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **BRUCHHAUS, Rainer** [DE/JP]; 2-12-35 Ushikubo-Higashi, Tsuzuki-ku, Yokohama-shi, Kanagawa 224-0014 (JP).

(74) Agent: **EPPING, HERMANN & FISCHER**; Ridlerstrasse 55, 80339 München (DE).

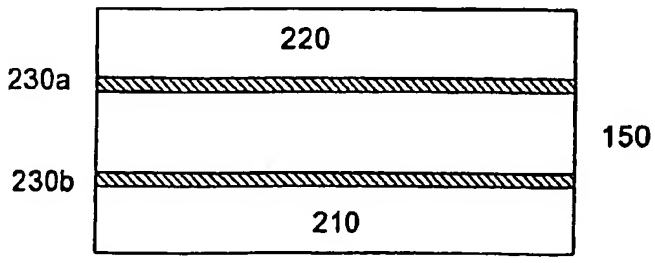
(81) Designated States *(national)*: CN, JP, KR, US.

(84) Designated States *(regional)*: European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: IMPROVED MATERIAL FOR USE WITH FERROELECTRICS



(57) Abstract: A liner layer comprising TiO_2 enriched SRO is disclosed. The TiO_2 enriched SRO liner improves the reliability of ferroelectric materials such as PZT without adversely impacting or degrading the ferroelectric properties of the PZT. The SRTO, in one embodiment is sputtered using an SRO target doped with 1-10% TiO_2.

WO 03/021656 A2

IMPROVED MATERIAL FOR USE WITH FERROELECTRICS

FIELD OF THE INVENTION

The present invention relates to ferroelectric integrated circuits and, more particularly, to materials that reduces fatigue in the ferroelectric material.

BACKGROUND OF THE INVENTION

Ferroelectric metal oxide ceramic materials such as lead zirconate titanate (PZT) have been investigated for use in ferrolectric semiconductor memory devices. A memory cell of the ferroelectric memory device includes a capacitor which serves as the storage element. Fig. 1 shows a conventional ferroelectric capacitor 101. As shown, the capacitor comprises a ferroelectric metal oxide ceramic layer 150 sandwiched between first and second electrodes 110 and 120. The electrodes typically are formed from a noble metal such as platinum.

The ferroelectric capacitor uses the hysteresis polarization characteristic of the ferroelectric material for storing information. The logic value stored in the memory cell depends on the polarization of the ferroelectric capacitor. To change the polarization of the capacitor, a voltage which is greater than the

to a performance degradation of the ferroelectric capacitor.

To counterbalance the loss of RuO_2 during crystallization, an SRO target with excess RuO_2 is used. However, the excess RuO_2 diffuses and reacts with the ferroelectric layer during high temperature crystallization of the ferroelectric material which degrades its ferroelectric properties.

From the foregoing discussion, it is desirable to provide an improved material which reduces fatigue without adversely impacting its ferroelectric properties.

SUMMARY OF THE INVENTION

The invention relates to the use of materials which reduces fatigue in ferroelectric materials without adversely affecting its ferroelectric properties. In one embodiment of the invention, the material comprises SRO which is enriched with TiO_2. The SRO comprises about 1-10 atomic weight percent (unless otherwise specified, all percentages are in atomic weight percent) of TiO_2. In one embodiment, the TiO_2 enriched SRO is formed on a substrate which is processed to include a first or bottom capacitor electrode. A ferroelectric material

such as PZT is formed on the TiO_2 enriched SRO. Subsequently, a second TiO_2 enriched SRO layer is formed on the ferroelectric layer followed by formation of the upper electrode. In one embodiment, the SRO enriched layer is formed by sputtering using an SRO target doped with 1-10 percent % TiO_2.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 shows a conventional ferroelectric capacitor;

Fig. 2 shows a ferroelectric capacitor in accordance with one embodiment of the invention;

Fig. 3 shows an illustrative system for depositing the TiO_2 enriched SRO layer in accordance with one embodiment of the invention; and

Fig. 4 shows an SRTO layer after a crystallization anneal.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 2 shows a ferroelectric capacitor 201 in accordance with one embodiment of the invention. Such a capacitor, for example, is used to form a ferroelectric memory cell of a ferroelectric memory IC. As shown, the capacitor comprises first and second electrodes 210 and

220. The electrodes are formed from, for example, platinum or a noble metal such as Ir, Pd, IrO_2 or other conducting oxides. A ferroelectric layer 150 is located between the electrodes. In one embodiment, the ferroelectric material comprises PZT or lead-lanthanum-zirconium-titanate (PLZT). Other types of ferroelectric material, such as Strontium-bismuth-tantalate (SBT) may also be used.

Liner layers 230a-b are provided between the electrodes and the ferroelectric layer to reduce fatigue in the ferroelectric layer. In accordance with the invention, the liner layer comprises TiO_2 enriched SRO (e.g., TiO_2 doped SRO). The TiO_2 increases the stability of the SRO layer which in turn, reduces the formation of flowerlike features. In one embodiment, the SRO is doped with 1-10 percent of TiO_2. Greater than 10% of TiO_2 in the SRO film can increase the sheet resistance of the TiO_2 enriched SRO layer beyond desirable limits, thus adversely impacting the performance of the capacitor. In one embodiment, the thickness of the TiO_2 enhanced SRO layer is about 5-50nm, the ferroelectric layer is about 100-200nm, and the electrode is about 10-100nm. The preferred thickness of the TiO_2 doped SRO is in the range

of 5-50 nm, typical PZT thicknesses are 100-200 nm, Pt 10-100 nm.

The TiO_2 enriched SRO layer is sputtered, in one embodiment, on the substrate. Fig. 3 shows a sputtering system 301 used to deposit the TiO_2 enriched SRO layer. The system includes a substrate support 305 on which a substrate is mounted. The substrate has been processed to include, for example, a conductive layer such as platinum to serve as the bottom electrode of the capacitor. Depending on the process, the conductive layer can be patterned or not. The system also includes a sputtering target 310 comprising a SRO ceramic compound enriched with 1-10 percent of TiO_2.

During the sputtering process, atoms from the target react to form an amorphous layer 330 consisting of SrO, TiO_2 and RuO_2 on the substrate. The parameters of the sputtering process, for example, are as follows:

Pressure: 0.5 -1 Pa

Temperature: room temperature to 650°C

Power: 500-1000 W

Reactive gas: Ar gas with 5 - 50 % volume weight %

After deposition, the amorphous film is crystallized by an annealing process at, for example, a temperature of 450 - 700°C for about 30 seconds to 5 minutes. During

the anneal, excess SrO is transformed into $SrTiO_3$ (STO). STO is a stable material having a perovskite structure similar to that of PZT and other types of ferroelectric materials. The TiO_2 enriched SRO layer may also contain unreacted TiO_2 grains 434, as shown in Fig. 4. The STO and unreacted TiO_2 grains serve as nucleation sites for the subsequently formed ferroelectric layer, triggering a very uniform grain structure in the ferroelectric layer and improved ferroelectric properties.

After the crystallization of the TiO_2 enriched SRO layer, the process continues to form the ferroelectric capacitor and completion of the IC. This, for example, includes forming the ferroelectric layer, the second TiO_2 enriched SRO layer, upper electrode, interconnects and interlevel dielectrics, passivation layer and packaging.

While the invention has been particularly shown and described with reference to various embodiments, it will be recognized by those skilled in the art that modifications and changes may be made to the present invention without departing from the spirit and scope thereof. The scope of the invention should therefore be determined not with reference to the above description but with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. A method for forming a ferroelectric capacitor comprising:

providing a substrate having a first conductive layer formed thereon, the first conductive layer serves as a electrode of the capacitor;

depositing a first amorphous liner layer on the electrode;

depositing a ferroelectric layer on the first liner layer;

depositing a second amorphous liner layer on the ferroelectric layer; and

depositing a second conductive layer on the liner layer, the second conductive layer serves as a second electrode, wherein the liner layer comprises SRO enriched about 1-10% TiO_2 weight percent, wherein the liner layers improve the properties of the ferroelectric layer.

2. The method of claim 1 wherein the ferroelectric layer comprises PZT.

3. The method of claim 2 wherein the first electrode comprises a noble metal.

4. The method of claim 3 wherein the first electrode comprises platinum.

5. The method of claim 1 wherein the electrodes comprise a noble metal.

6. The method of claim 5 wherein the electrodes comprise platinum.

7. The method of claim 1,2,3,4,5 or 6 further comprises an annealing process to crystallize the TiO_2 enriched SRO layer.

8. The method of claim 7 wherein the annealing process comprise heating the TiO_2 enriched SRO layer at a temperature of about 650°C for about 30 sec.

9. The method of claim 8 further comprising the steps for completing a ferroelectric memory IC.

10. The method of claim 7 further comprising the steps for completing a ferroelectric memory IC.

11. A method for forming a ferroelectric capacitor comprising:

depositing a first amorphous layer on a substrate;

depositing a ferroelectric layer on the first liner layer;

depositing a second amorphous liner layer on the ferroelectric layer; and

depositing a second conductive layer on the liner layer, the second conductive layer serves as a second electrode, wherein the liner layer comprises SRO enriched with about 1-10% TiO_2, wherein the liner layers improves the properties of the ferroelectric layer.

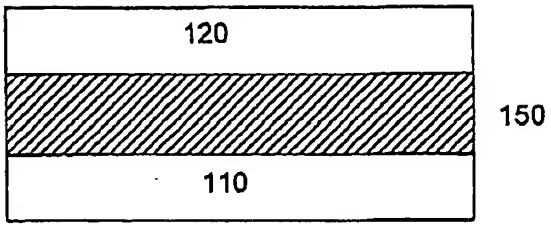
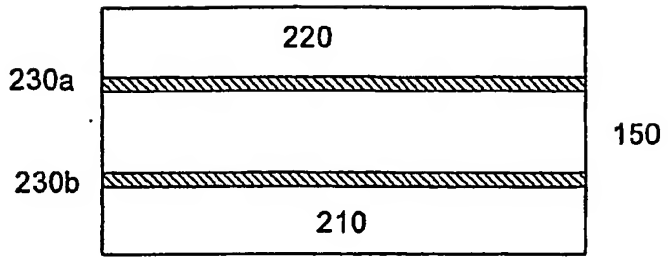


Fig. 1

PRIOR ART



201

Fig. 2

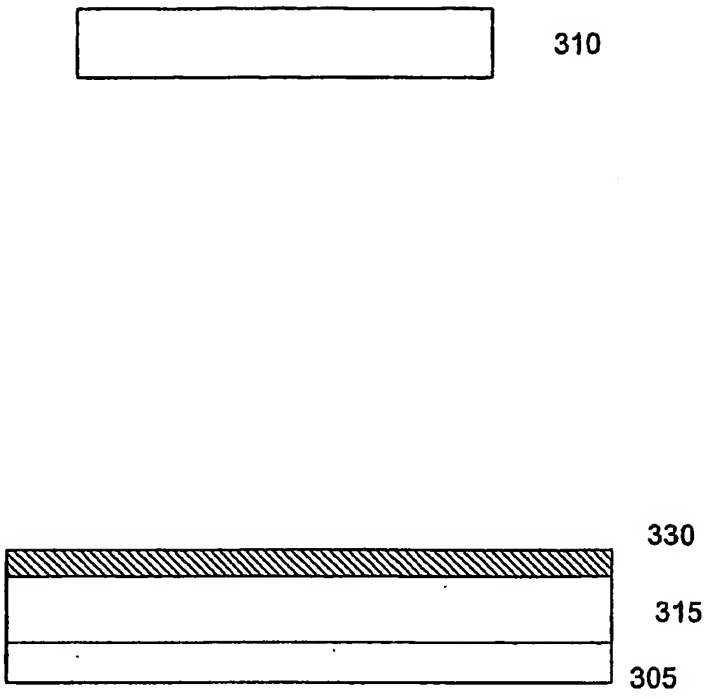


Fig. 3

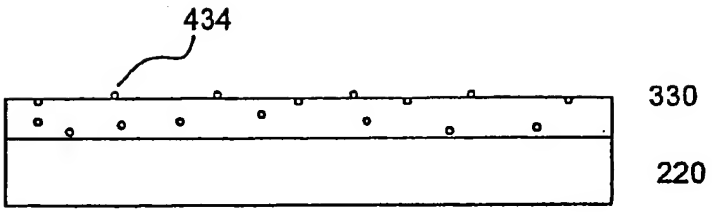


Fig. 4